

FIG. 1

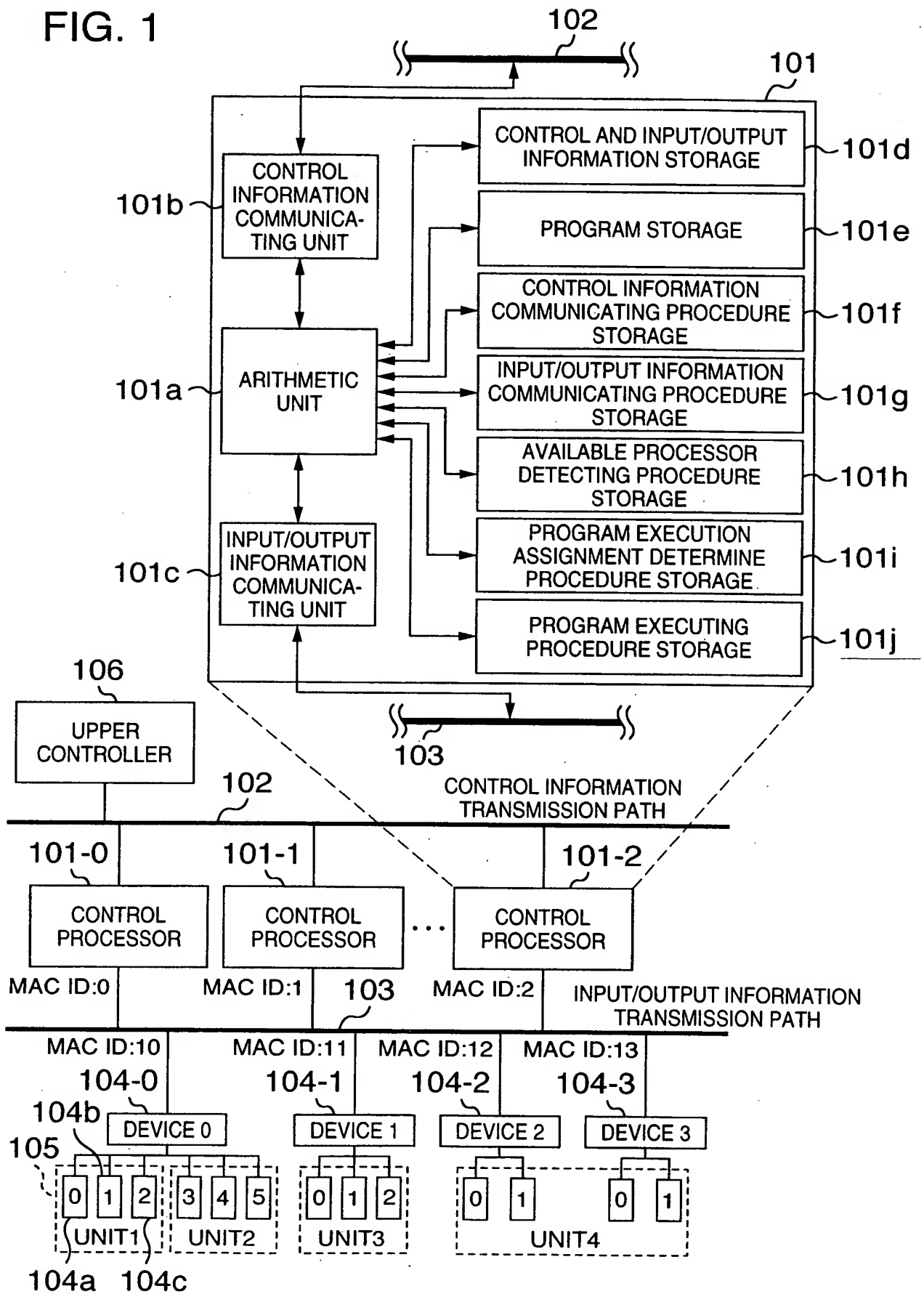


FIG. 2

201 LOGICAL PORT NO.	202a PHYSICAL PORT NO.	
	MAC ID	202 PORT NO. 202b
0	10	0
1	10	1
2	10	2
3	10	3
4	10	4
5	10	5
6	11	0
7	11	1
8	11	2
9	12	0
10	12	1
11	13	0
12	13	1

FIG. 3

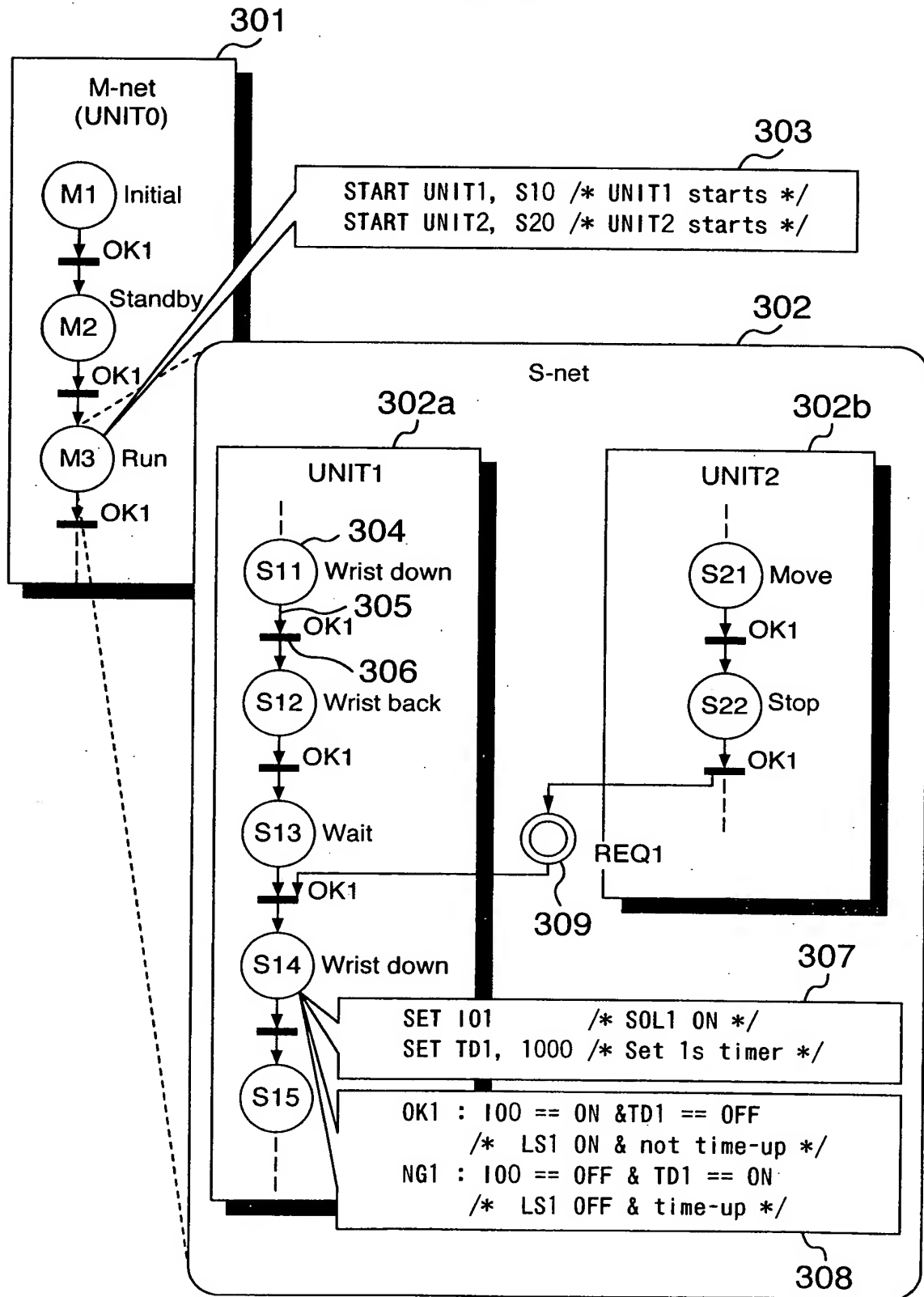


FIG. 4

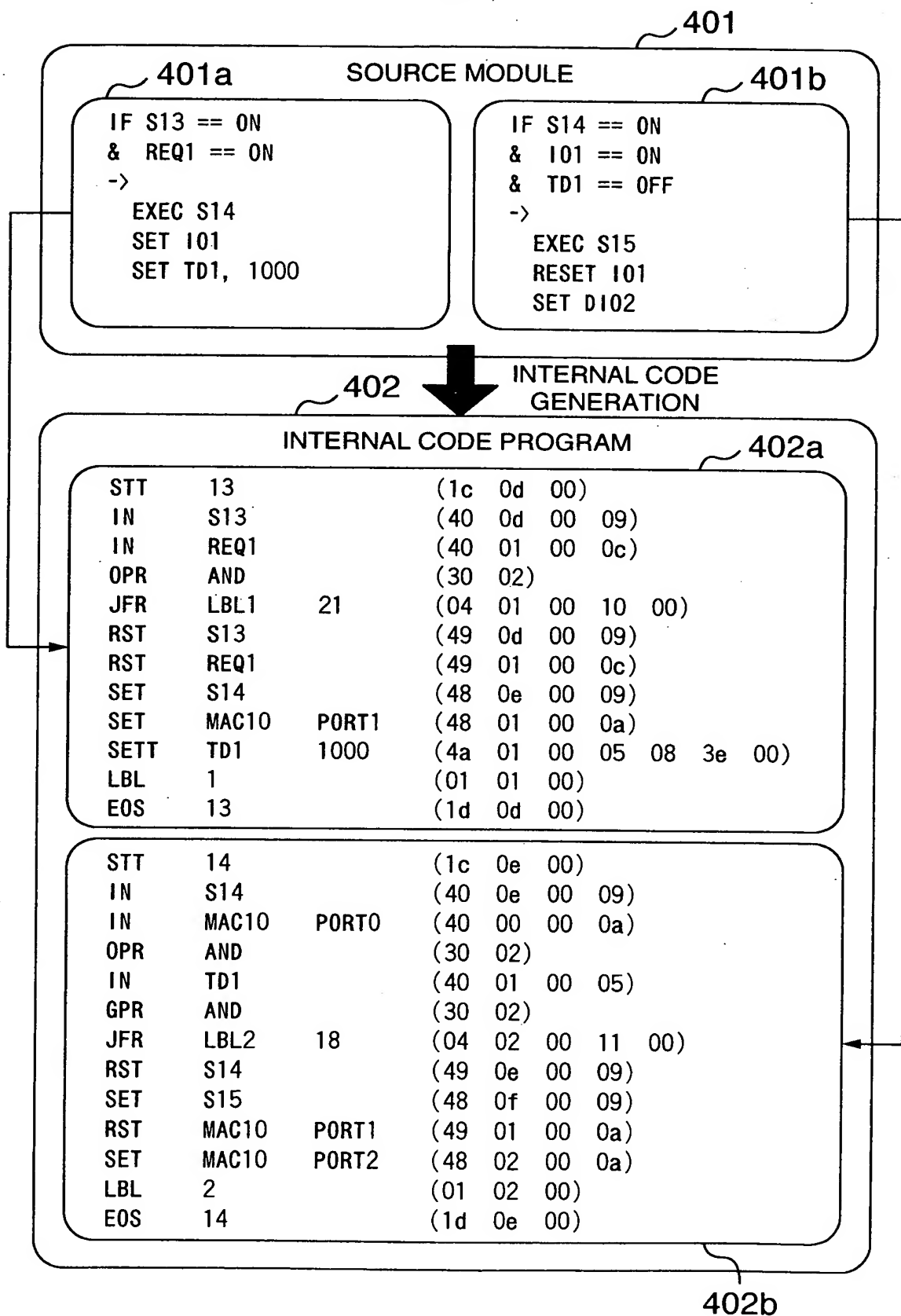


FIG. 5

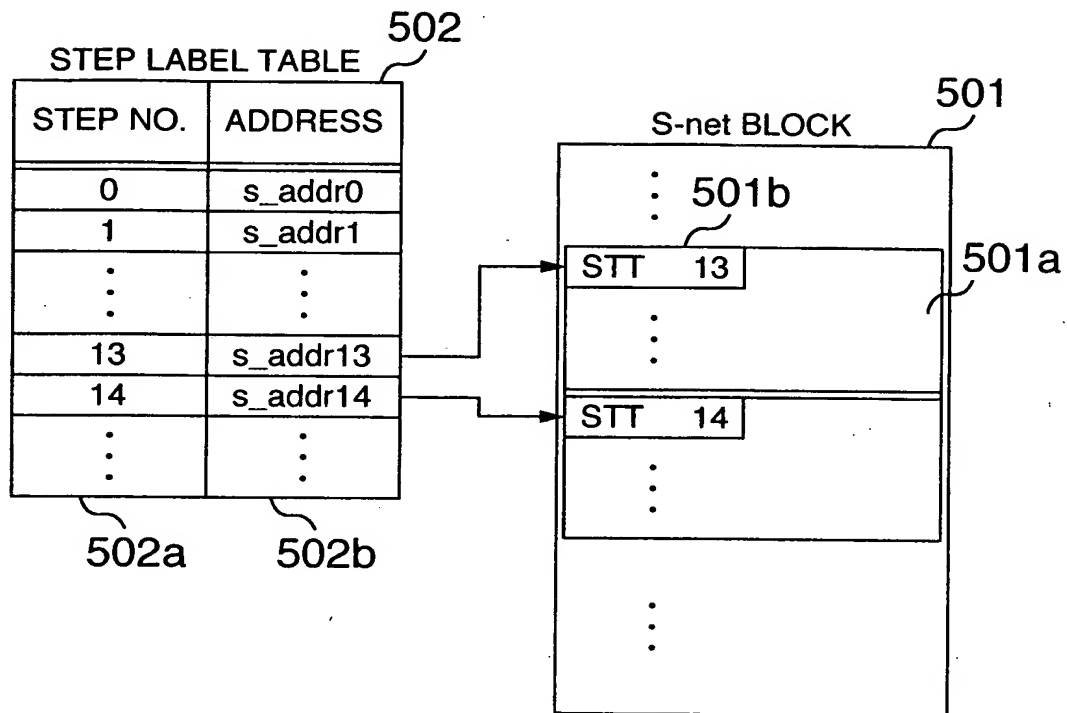


FIG. 6

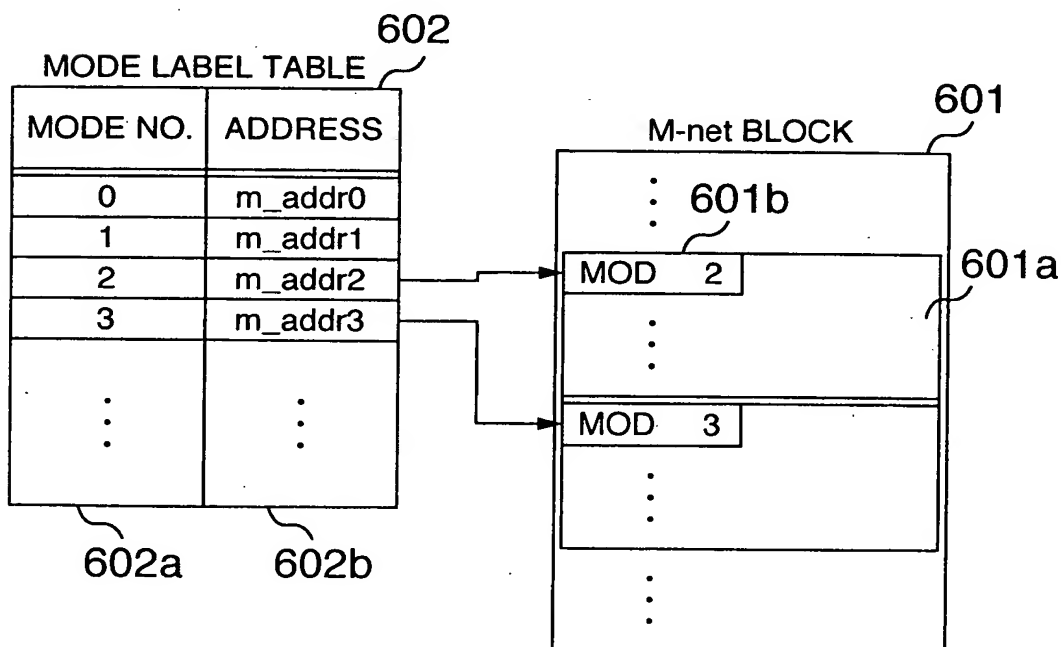


FIG. 7

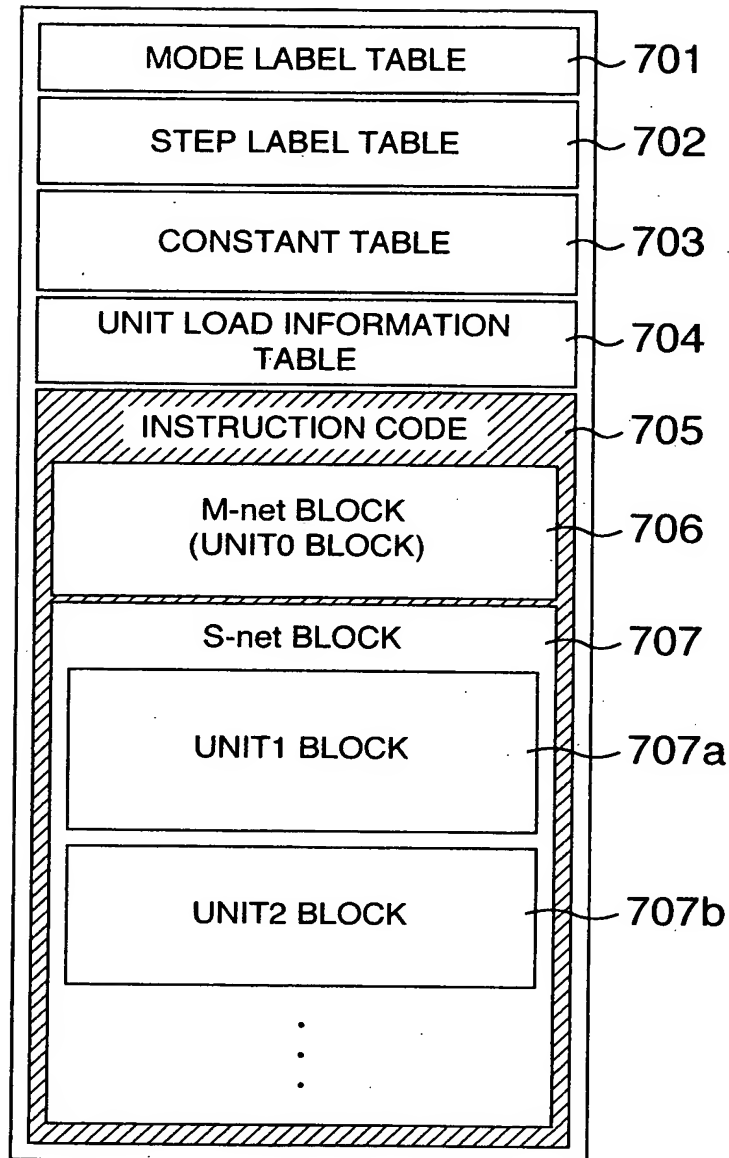


FIG. 9

901 PROCESSOR NO.	902 MAC ID	903 PROCESSOR TYPE
0	0	A
1	1	A
2	2	B

FIG. 8

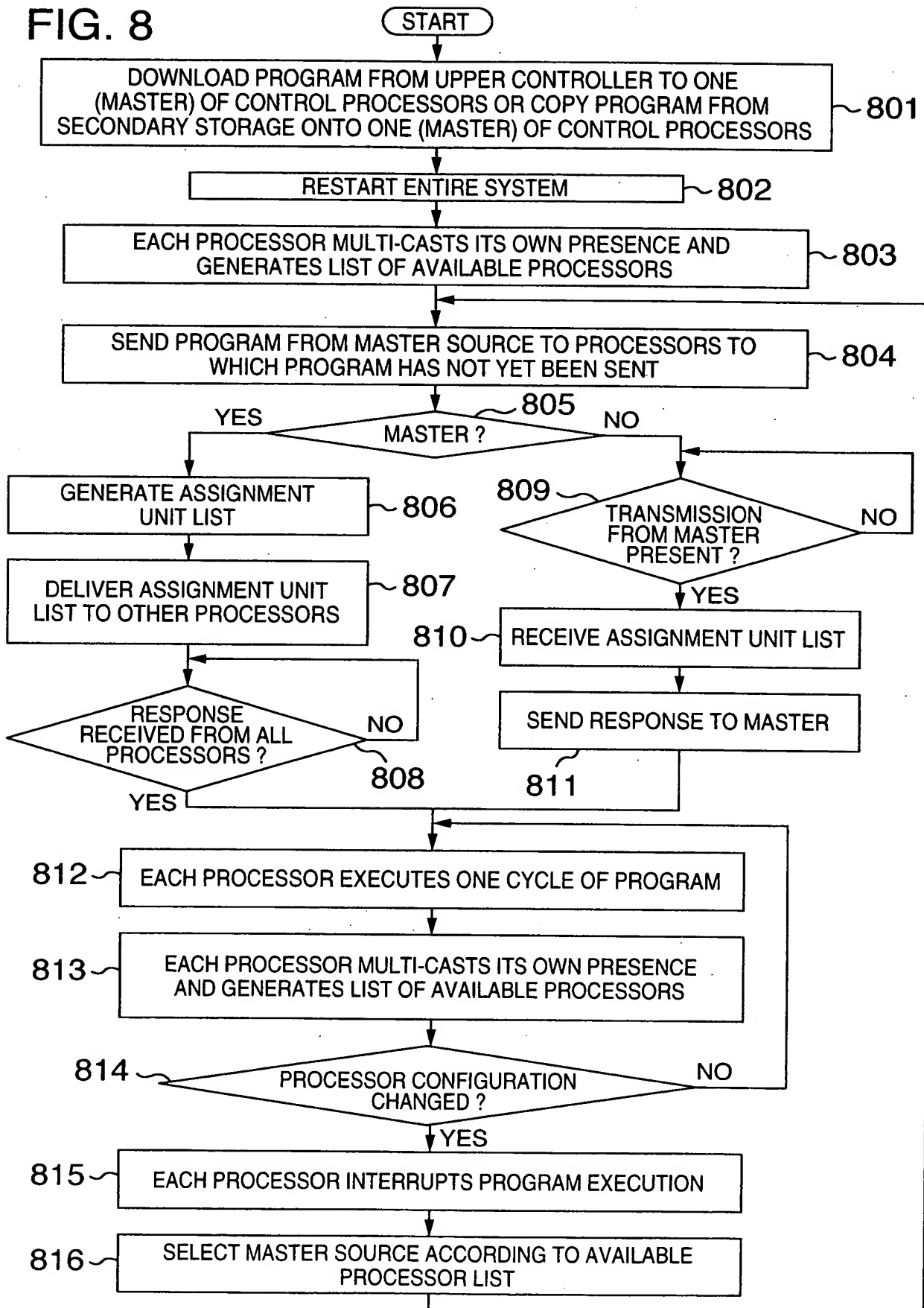


FIG. 10

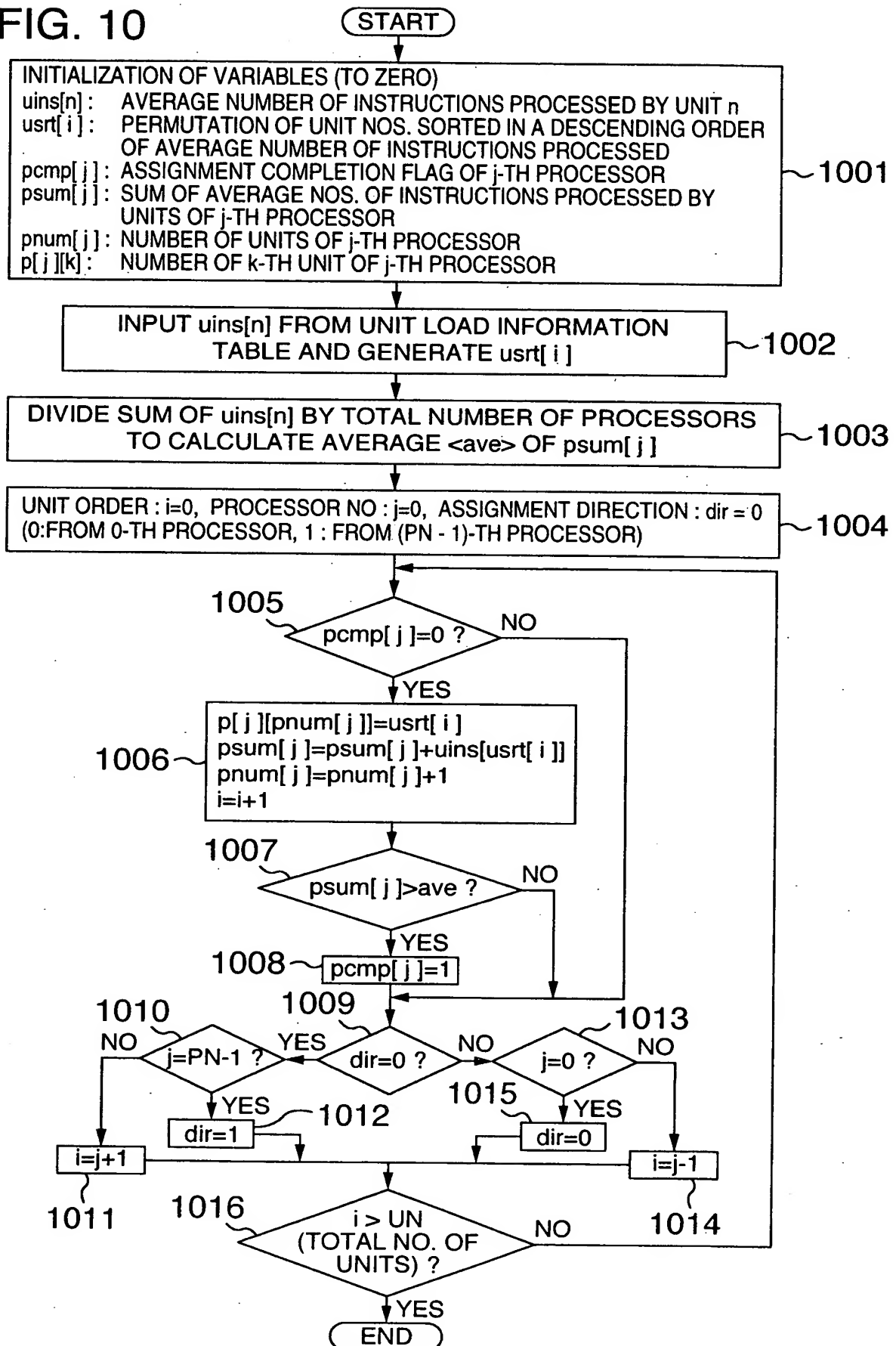


FIG. 11

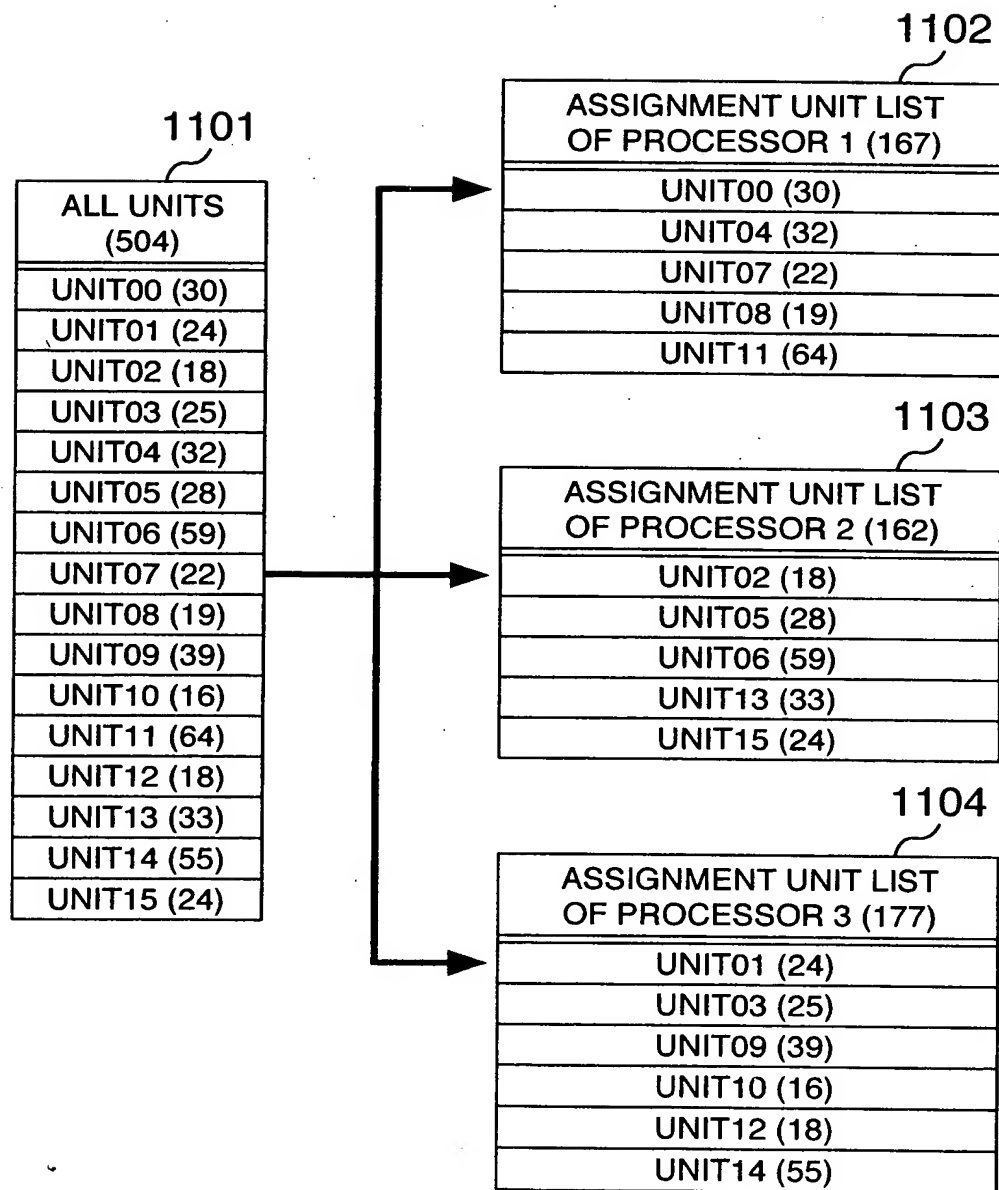


FIG. 12

1201		1202	
UNIT NO.	STEP NO.	SYNCHRONIZA- TION PLACE NO.	STATE
0	3	0	OFF
1	16	1	OFF
2	21	2	ON
1201a	1201b	1202a	1202b

1203	
VARIABLE NO.	VALUE
0	value0
1	value1
2	value2
1203a	1203b

FIG. 13

1301		
MAC ID	PORT NO.	STATE
10	0	OFF
	1	ON
	2	OFF
11	0	OFF
	1	ON
	2	ON
1301a	1301b	1301c

FIG. 14

